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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,484	10/16/2003	Yuh-Turng Liu	681939-65US	5382

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AKIN GUMP STRAUSS HAUER & FELD L.L.P.
ONE COMMERCE SQUARE
2005 MARKET STREET, SUITE 2200
PHILADELPHIA, PA 19103

EXAMINER	
PHAM, THANH V	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/685,484	**Applicant(s)** LIU ET AL.	
	Examiner Thanh V. Pham	**Art Unit** 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment overcomes the objection stated in the previous Office action.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-2, 4-12, 14-17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong US 6,465,351 B1 in combination with Mikolas US Pub. 2004/0005769 A1.

Re claims 1, 12 and 17, the Jeong reference discloses a method of manufacturing a semiconductor device comprising the steps of:

providing a semiconductor wafer 200 including a patterned layer 206;

forming a first insulating layer 216 over the patterned layer of the semiconductor wafer, the first insulating layer 216 is conformal with the patterned layer 206 (fig. 1C, *re claim 4*), the first insulating layer 216 is silicon nitride (col. 8, line 36, *re claims 5 and 14*) *inherently* including a first index of refraction;

forming a second insulating layer 218 over the first insulating layer 216, the second insulating layer 218 of silicon oxide (col. 8, line 46, *re claim 6*) *inherently* including a second index of refraction (of silicon oxide 218) smaller than the first index of refraction (of silicon nitride 216);

removing the second insulating layer 218 by a planarizing process (col. 8, line 65 – col. 9, line 3, *re claim 8*);

The Jeong reference discloses the first insulating layer 216 as "the CMP stopping layer to serve for CMP end point detection" (col. 2, line 15) **but** does not clearly state how the planarizing step is ceased (*re claim 2 and the last steps of claims 12 and* 17) and **lacks** the step of detecting a change in index of refraction *between the first insulating layer and the second insulating layer* **during** the planarizing process.

The Mikolas reference discloses

> (Abstract) ... methods of detecting a planarization endpoint in chemical mechanical planarization of a substrate wherein a detectable target is located at the endpoint and then detected during the CMP planarization.
> [0006] ... whether the substrate surface has been planarized to a desired flatness or thickness or whether the surface material has been removed from the substrate.
> [0007] ... monitoring a parameter associated with the substrate surface, and indicating an endpoint when the parameter abruptly changes.
> [0013] ... the systems of the present invention can utilize multiple targets to provide increased accuracy. The targets can possess different properties thus warning of the approach of different events, such as layer breakthrough. The data collected may be in the form of a count rate above a certain threshold, thus it is simple to process and there is no spectral analysis required for the data, the targets of the invention are compatible with VLSI. Endpointing is measured in real time while the wafer is in motion thus providing virtually instantaneous feedback. The optics used for detection of signals can be very small in size thus facilitating incorporation of the system into a planarization machine.
> [0027] ... a "first layer" and a "second layer" can both be dielectric layers of different materials.
> [0029] ... the term "target" refers to one or more structures that can be detected by a detection system... the target is a compound or compounds that undergo a detectable change in response to light ... and/or other energy absorbing compound.
> [0030] ... the phrase "detecting the target" and observing the target" are used interchangeably and include detecting or observing the presence or absence or removal of the target ... The target is determined from an interpretation of the instantaneous optical intensity of the diffracted light level as the target passes through the field of view.
> [0040] The target used in the invention is any detectable structure that can be detected at its location by a suitable detection system ... it can be a spectrally active material.

> [0044] .. first and second layers (12, 11) preferably have different planarization removal rates... provided that the index of refraction of the other layer is substantially different from the first layer and the CMP slurry, thus providing an observable optical effect.
> [046] Chemical mechanical planarization of the uneven top surface (15) of the second layer (11) results in a planar top surface (15), as shown in FIG. 1B, in which the grating is either optically invisible (if the indices of refraction of the layers are essentially equal) or is visible but does not change during the planarization step. Continued planarization of the second layer (11) results in almost complete removal of the second layer 11, as shown in FIG. 1C.
> [0047] Further planarization results in additional removal of the top layer and formation of a wash board topography produced by short range dishing (16), resulting from the different rates at which the first and second materials are removed from the substrate by CMP, as discussed above and as shown in FIG. 1D.
> [0056] If two adjacent material layers (for example, (11) and (12) in FIG. 1) possess substantially the same indices of refraction and CMP removal rates, then it will be difficult to observe ...

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of Jeong with the endpoint detection method disclosed in Mikolas to have the step of detecting a change in index of refraction between the first insulating layer and the second insulating layer during the planarizing process since the endpoint detection of Mikolas would provide the manufacturing process of Jeong with “accurately and reliably indicate when the planarization process is complete” (Mikolas' [0009]).

Re claims 7 and 15, with silicon nitride for the first insulating film 216 and silicon oxide for the second insulating film 218, the Jeong reference *inherently* provides (known inherency/characteristics in US Pub. 2005/0031789 A1's table 4) the first insulating layer with a first removal rate and the second insulating layer with a second removal rate greater than the first removal rate and adjusting the additive agents would yield the second removal rate being approximately three time the first removal rate (*re claim 16*); and also, *re claims 9-10*, (known characteristics in US Pub. 2005/0045979 A1's [0068]) the first index of refraction of silicon nitride is 2.07 and the second index of refraction of silicon nitride is 1.47.

Re claim 11, the Jeong reference further discloses a step of forming an oxide layer 214 (col. 8, line 24) over the patterned layer 206 of the semiconductor wafer 200 before forming the first insulating layer 216 (fig. 1C).

Re claim 19, the Mikolas reference further discloses the three detection systems with a monitor, figs. 6-8.

4. Claims 3, 13 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong in combination with Mikolas as applied to claims 1-2, 4-12, 14-17 and 19 above, and further in view of Dawson et al. US 5,516,729.

The combination discloses substantially all of the instant invention but lacks the step of removing a portion of the first insulating layer by the planarizing process when the change in index of refraction is detected or the endpoint is determined.

The Dawson et al. reference discloses methods for planarizing a semiconductor topography comprising providing a semiconductor surface including a patterned layer 31, fig. 3; forming a first insulating layer 32 over the patterned layer, the first insulating layer including a first index of refraction; forming a second insulating layer 38 over the first insulating layer, the second insulating layer including a second index or refraction; removing the second insulating layer by planarizing process wherein the first and the second removals remove the second insulating layer, the third and the fourth removals remove further the first insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the combination of Jeong and Mikolas with the further removal of the first insulating layer of Dawson et al. because the further removal of Dawson et al. would provide the combination process of Jeong and Mikolas with a profile slightly elevated from the upper surface of the patterned layer (Dawson's col. 7, lines14-15). Alternately, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the structure of Dawson et al. with the combination process of Jeong and Mikolas because the process of the combination would provide the structure formation of Dawson et al. with index detection or endpoint determination for accurate and reliable CMP.

Response to Arguments

5. Applicant's arguments filed 08/25/2005 have been fully considered but they are not persuasive.

6. With the added limitation "between the first insulating layer and the second insulating layer", applicant argues that the combination of Jeong and Mikolas does not discloses the step of detecting a change of index of refraction between the first insulating layer and the second simulating layer during the planarization. The examiner further quotes some more passages in Mikolas to show that limitation in the rejection.

The added limitation "between the first insulating layer and the second insulating layer" is considered as inherently performed during the planarizing process, the detecting step is understood as continuously detecting a change in indexes of refraction as described in Mikola's [0013]. Otherwise, this added limitation might be rejected under 35 USC 112 as lacking support in the specification. The pointed to paragraph as discussed in the Remark's page 6 (instant specification's [0024]) or the instant specification does not have this limitation.

7. The argument on the rejection under 35 USC 103 is the same and responded as the above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-T (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/03/2005

George Fourson
Primary Examiner